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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/695,839	10/29/2003	Makoto Matsushima	2271/71352	7847

7590 05/09/2007
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EXAMINER

PHU, PHUONG M

ART UNIT	PAPER NUMBER
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2611

MAIL DATE	DELIVERY MODE
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05/09/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/695,839

Applicant(s)

MATSUSHIMA, MAKOTO

Examiner

Phuong Phu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5, 6, 8-10 and 12 is/are rejected.
- 7) ☒ Claim(s) 4, 7 and 11 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is responsive to the Amendment filed on 3/26/07. Accordingly, claims 1-12 are currently pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5, 6, 8-10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Kudo et al (6,658,583).

-Regarding to claim 1, Kudo et al discloses a PWM signal generating circuit (see figure 1B) comprising:

a first counter circuit (902, 904, 906) of periodically changing a PWM signal output (PWM SIGNAL) therefrom into an active state by changing the PWM signal output from L-level to H-level (see figures 1B, 1C, col. 1, lines 19-34); and

a second counter circuit (902, 900, 908) of changing the PWM signal, which has been changed into the active state by said first counter circuit, into an inactive state within each cycle by changing the PWM signal output from H-level to L-level, wherein said second counter circuit comprises element (900) to increase and decrease an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state (see figures 1B, 1C, col. 1, lines 15-43).

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-Regarding to claim 2, Kudo et al discloses that the PWM signal circuit consists of a plurality of circuit elements (900, 902, 904, 908, 906, 909), each of which outputs a digital signal (see figure 1B).

-Regarding to claim 3, Kudo et al discloses a first specifying circuit (900, 904) (see figure 1B) that specifies an upper limit value (910) (see figure 1C) and a lower limit value (see figure 1C), wherein said second counter circuit changes the active-to-inactive time period periodically within a range between the upper limit value and the lower limit value (see col. 1, lines 15-43).

-Regarding to claim 12, in Kudo et al, said second counter circuit determines the falling edges (912) (see figure 1C) of the PWM signal output, and in associated with the rising edges (910), the falling edges, therefore, make the pulse width of the PWM signal output increased or decreased (inherently at a certain rate) in a time period/interval (as shown in figure 1A) (see col. 1, lines 12-42). Or namely, it can be said that the second counter circuit increases or decreases the time period, (being the pulse width of the PWM signal), between the time (occurred at the rising edges) when the PWM signal is changed into the active state and the time (occurred at the falling edges) when the PWM signal is changed into the inactive state, at a predetermined rate in a predetermined period.

-Regarding to claim 5, as similarly applied to claims 1-3, set forth above and herein incorporated, Kudo et al discloses a method (see figures 1B and 1C) of generating a PWM signal (PWM SIGNAL), comprising:

procedure (902, 904, 906) (see figure 1B) of periodically changing the PWM signal into an active state; and

procedure (902, 900, 908) (see figure 1B) of changing the PWM signal, which has been changed into the active state, into an inactive state within each cycle, while changing an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

-Regarding to claim 6, Kudo et al discloses procedure (900, 904) (see figure 1B) of changing the active-to-inactive time period periodically within a range between an upper limit value (910) (see figure 1C) and a lower limit value (see figure 1C).

-Regarding to claim 8, similarly applied to claims 1-3, set forth above and herein incorporated, Kudo et al discloses a PWM signal generating circuit (see figure 1B) comprising:

first counter means (902, 904, 906) for periodically changing a PWM signal output (PWM SIGNAL) therefrom into an active state; and

second counter means (902, 900, 908) for changing the PWM signal, which has been changed into the active state by said first counter means, into an inactive state within each cycle, wherein said second counter means increases and decreases an active-to-inactive time period from a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

-Claim 9 is rejected with similar reasons set forth for claim 2.

-Claim 10 is rejected with similar reasons set forth for claim 3.

Allowable Subject Matter

4. Claims 4, 7 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed on 3/26/07 have been fully considered but they are, in part, not persuasive.

-The rejections under 35 USC 112, second paragraph, to claims 2 and 9, have been withdrawn since the claims were amended and overcame the rejection.

- Applicant's arguments, with respect to the rejection to claim 1 as being anticipated by Kudo et al, are not persuasive. The applicant mainly argues that Kudo et al does not teach or suggest a PWM signal generating circuit comprising a first counter circuit periodically changing a PWM signal output therefrom into an active state; and a second counter circuit changing the PWM signal, which has been changed into the active state by said first counter circuit, into an inactive state within each cycle, wherein said second counter circuit increases and decreases a time period between a time when the PWM signal is changed into the active state to a time when the PWM signal is changed into the inactive state.

The examiner respectfully disagrees. Note that the rejection is based on the limitations recited in the claim. Kudo et al discloses a PWM signal generating circuit (see figure 1B), (considered here equivalent with the limitation "PWM signal generating circuit"), comprising:

a first counter circuit (902, 904, 906) (see figure 1B), (considered here equivalent with the limitation "first counter circuit"), of periodically changing a PWM signal output (PWM SIGNAL) therefrom into an active state by changing the PWM signal output from L-level to H-level in such a way that for each period of the PWM signal, the first counter circuit specifies and sets the rising edge (910) (see figure 1C) of the PWM signal for changing the PWM signal

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output from L-level to H-level, or namely, changing the PWM from an inactive state (being the L-level) into an active state (being the H-level) (see col. 1, lines 12-43); and

a second counter circuit (902, 900, 908) (see figure 1B), (considered here equivalent with the limitation "second counter circuit"), of changing the PWM signal, which has been changed into the active state by said first counter circuit, into an inactive state within each cycle by changing the PWM signal output from H-level to L-level in such a way that for each period of the PWM signal, the second counter circuit specifies and sets the falling edge (912) (see figure 1C) of the PWM signal for changing the PWM signal, which has been changed into the active state (being the H-level) by said first counter circuit, into an inactive state (being the L-level) by changing the PWM signal from the H-level to the L-level (see col. 1, lines 12-43);

wherein said second counter circuit increases and decreases a time period, (being the pulse width of the PWM signal), between a time (occurred at the rising edges) when the PWM signal is changed into the active state (being the H-level) to a time (occurred at the corresponding falling edges) when the PWM signal is changed into the inactive state (being the L-level) in such a way that in Kudo et al, said second counter circuit determines the falling edges (912) (see figure 1C) of the PWM signal output, and in associated with the rising edges (910), the falling edges, therefore, make the pulse width of the PWM signal increased or decreased in a time interval (as shown in figure 1A) (see col. 1, lines 12-43).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (8:00 AM - 4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Phuong Phu
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05/03/07

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PRIMARY EXAMINER**

Phuong Phu
Primary Examiner
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